Claims:

1. An IC design planning method comprising the steps of:

providing a block placement representation being descriptive of an IC design, the IC design comprising a block having a block boundary and a plurality of sub-blocks being arranged within the block boundary, each of the plurality of sub-blocks having at least one pin and a sub-block boundary defining the area thereof, and the at least one pin of each of the plurality of sub-blocks having a positional arrangement;

positioning each of the at least one pin of each of the plurality of sub-blocks at a preliminary pin position along the block boundary of the block;

determining at least one sub-block placement parameter for each of the plurality of sub-blocks from the at least one external pin;

rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks, wherein at least a portion of the sub-block boundary of each of the plurality of sub-blocks coincides with at least one of a portion of the block boundary of the block and a portion of the sub-block boundary of another one of the plurality of sub-blocks; and

repositioning each of the at least one pin of each of the plurality of sub-blocks at a final position, the final position being a point on the sub-block boundary of the corresponding one of the plurality of sub-blocks being nearest to the preliminary position of the corresponding one of the at least one pin thereof.

2. The method as in claim 1, the step of providing the block placement representation comprising the step of providing the block placement representation generated by an optimization algorithm applied to the IC design.

3. The method as in claim 1, the step of providing the block placement representation comprising the step of providing the block placement representation generated by a genetic algorithm applied to the IC design.

4. The method as in claim 1, the step of positioning each of the at least one pin of each sub-block at a preliminary pin position along the block boundary of the block comprising the steps of:

obtaining a net of the IC design, the net being descriptive of at least one electrical path and signal passage thereon between one source pin and at least one sink pin, the source pin being one of the at least one pin of one of the plurality of sub-blocks and each of the at least one sink pin being one of the at least one pin of one of the plurality of sub-blocks;

finding a center of mass from the at least one sink pin;

positioning the source pin to a position on the block boundary of the block having the shortest distance from the center of mass of the at least one sink pin; and

positioning each of the at least one sink pin at a position on the block boundary of the block having the shortest distance from the position of the source pin,

wherein the preliminary position of each of the at least one pin of each of the plurality of sub-blocks is established in response to the source pin and the at least one sink pins being positioned.

5. The method as in claim 4, the step of obtaining a net of the IC design comprising the step of identifying at least one critical pin of the IC design, each of the at least one critical pin being associated with one of the at least one electrical path having a specific timing budget.

6. The method as in claim 1, the step of determining at least one sub-block placement parameter comprising the step of:

determining at least one of the orientation, the center of mass and the weight of the at least one pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof to thereby determine the at least one sub-block placement parameter of one of the plurality of sub-blocks therefrom.

7. The method as in claim 6, the step of determining at least one of the orientation, the center of mass and the weight of the at least one pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof comprising the step of:

determining the weight of the at least one pin from the quantity of the at least one pin of the corresponding one of the plurality of sub-blocks.

8. The method as in claim 7, the step of determining the weight of the at least one pin from the quantity of the at least one pin of the corresponding one of the plurality of sub-blocks comprising the step of determining the weight of the at least one critical pin from the quantity of the at least one critical pin of the corresponding one of the plurality of sub-blocks, each of the at least one critical pin being associated with an electrical path having a specific timing budget, the electrical path being described in a net of the IC design.

9. The method as in claim 6, the step of determining at least one of the orientation, the center of mass and the weight of the at least one pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof comprising the steps of:

bounding the at least one pin of each of the plurality of sub-blocks with a rectangle having an area, wherein the area of the rectangle being dimensioned for bounding the at least one pin of each of the plurality of sub-blocks is minimised; and

determining the angle between the longest side of the rectangle of each of the plurality of sub-blocks and the horizontal axis of the block to thereby determine the orientation of the at least one pin of the corresponding one of the plurality of sub-blocks, and the orientation of the at least one pin being one of horizontal, partially horizontal, vertical, and partially vertical.

10. The method as in claim 1, the step of rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks comprising the step of:

determining a rearrangement sequence based on the determined at least one placement parameter of each of the plurality of sub-blocks; and

sequential altering the dimensions of one of the plurality of sub-blocks to facilitate repositioning of the corresponding one of the plurality of sub-blocks within the block boundary of the block in accordance with the rearrangement sequence.

11. The method as in claim 1, the step of rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks comprising the steps of:

selecting a block partition for the block, the block partition being one of a vertical block partition comprising a left block portion and a right block portion, and a horizontal block partition comprising a top block portion and a bottom block portion;

calculating a sub-block placement value for each of the plurality of sub-blocks based on the at least one sub-block placement parameter thereof, the sub-block placement value being algorithmically dependent upon the selected one of the top, bottom, left and right block partitions; and

selecting one of the plurality of sub-blocks for placement within the one of the top, bottom, left and right portions that the sub-block placement value of the selected one of the plurality of sub-blocks is algorithmically dependent upon, the selected one of the plurality of sub-blocks having the highest sub-block placement value.

12. An IC design planning method comprising the steps of:

providing a block placement representation being descriptive of an IC design, the IC design comprising a block having a block boundary and a plurality of sub-blocks being arranged within the block boundary, each of the plurality of sub-blocks having at least one external pin, at least one internal pin and a sub-block boundary defining the area thereof, and each of the at least one external pin and the at least one internal pin of each of the plurality of sub-blocks having a positional arrangement;

positioning each of the at least one external pin of each of the plurality of sub-blocks at a preliminary pin position along the block boundary of the block;

determining at least one sub-block placement parameter for each of the plurality of sub-blocks from the at least one external pin and the at least one internal pin;

rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks, wherein at least a portion of the sub-block boundary of each of the plurality of sub-blocks coincides with at least one of a portion of the block boundary of the block and a portion of the sub-block boundary of another one of the plurality of sub-blocks; and

repositioning each of the at least one external pin of each of the plurality of sub-blocks at a final position, the final position being a point on the sub-block boundary of the corresponding one of the plurality of sub-blocks being nearest to the preliminary position of the corresponding one of the at least one external pin thereof.

13. The method as in claim 12, the step of providing the block placement representation comprising the step of providing the block placement representation generated by an optimization algorithm applied to the IC design.

14. The method as in claim 12, the step of providing the block placement representation comprising the step of providing the block placement representation generated by a genetic algorithm applied to the IC design.

15. The method as in claim 12, wherein the step of positioning each of the at least one external pin of each sub-block at a preliminary pin position along the block boundary of the block comprising the steps of:

obtaining a net of the IC design, the net being descriptive of at least one electrical path and signal passage thereon between one source pin and at least one sink pin, the source pin being one of the at least one external pin of

one of the plurality of sub-blocks and each of the at least one sink pin being one of the at least one external pin of one of the plurality of sub-blocks;

finding a center of mass from the at least one sink pin;

positioning the source pin to a position on the block boundary of the block having the shortest distance from the center of mass of the at least one sink pin; and

positioning each of the at least one sink pin at a position on the block boundary of the block having the shortest distance from the position of the source pin,

wherein the preliminary position of each of the at least one external pin of each of the plurality of sub-blocks is established in response to the source pin and the at least one sink pins being positioned.

16. The method as in claim 15, the step of obtaining a net of the IC design comprising the step of identifying at least one critical pin of the IC design, each of the at least one critical pin being associated with one of the at least one electrical path having a specific timing budget.

17. The method as in claim 12, the step of determining at least one sub-block placement parameter comprising the step of:

determining at least one of the orientation, the center of mass and the weight of the at least one external pin and the weight of the at least one internal pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof to thereby determine the at least one sub-block placement parameter of one of the plurality of sub-blocks therefrom.

18. The method as in claim 17, the step of determining at least one of the orientation, the center of mass and the weight of the at least one external pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof comprising the step of:

determining the weight of the at least one external pin from the quantity of the at least one external pin of the corresponding one of the plurality of sub-blocks.

19. The method as in claim 18, the step of determining the weight of the at least one external pin from the quantity of the at least one external pin of the corresponding one of the plurality of sub-blocks comprising the step of determining the weight of the at least one critical pin from the quantity of the at least one critical pin of the corresponding one of the plurality of sub-blocks, each of the at least one critical pin being associated with an electrical path having a specific timing budget, the electrical path being described in a net of the IC design.

20. The method as in claim 17, the step of determining at least one of the orientation, the center of mass and the weight of the at least one external pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof comprising the steps of:

bounding the at least one external pin of each of the plurality of sub-blocks with a rectangle having an area, wherein the area of the rectangle being dimensioned for bounding the at least one external pin of each of the plurality of sub-blocks is minimised; and

determining the angle between the longest side of the rectangle of each of the plurality of sub-blocks and the horizontal axis of the block to thereby determine the orientation of the at least one external pin of the corresponding one of the plurality of sub-blocks, and the orientation of the at least one external pin being one of horizontal, partially horizontal, vertical, and partially vertical.

21. The method as in claim 12, the step of rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks comprising the step of:

determining a rearrangement sequence based on the determined at least one placement parameter of each of the plurality of sub-blocks; and

sequential altering the dimensions of one of the plurality of sub-blocks to facilitate repositioning of the corresponding one of the plurality of sub-blocks within the block boundary of the block in accordance with the rearrangement sequence.

22. The method as in claim 12, the step of rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks comprising the steps of:

selecting a block partition for the block, the block partition being one of a vertical block partition comprising a left block portion and a right block portion, and a horizontal block partition comprising a top block portion and a bottom block portion;

calculating a sub-block placement value for each of the plurality of sub-blocks based on the at least one sub-block placement parameter thereof, the sub-block placement value being algorithmically dependent upon the selected one of the top, bottom, left and right block partitions; and

selecting one of the plurality of sub-blocks for placement within the one of the top, bottom, left and right portions that the sub-block placement value of the selected one of the plurality of sub-blocks is algorithmically dependent upon, the selected one of the plurality of sub-blocks having the highest sub-block placement value.

23. An IC design planning system comprising:

means for providing a block placement representation being descriptive of an IC design, the IC design comprising a block having a block boundary and a plurality of sub-blocks being arranged within the block boundary, each of the plurality of sub-blocks having at least one pin and a sub-block boundary defining the area thereof, and the at least one pin of each of the plurality of sub-blocks having a positional arrangement;

means for positioning each of the at least one pin of each of the plurality of sub-blocks at a preliminary pin position along the block boundary of the block;

means for determining at least one sub-block placement parameter for each of the plurality of sub-blocks from the at least one external pin;

means for rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks, wherein at least a portion of the sub-block boundary of each of the plurality of sub-blocks coincides with at least one of a portion of the block boundary of the block and a portion of the sub-block boundary of another one of the plurality of sub-blocks; and

means for repositioning each of the at least one pin of each of the plurality of sub-blocks at a final position, the final position being a point on the sub-block boundary of the corresponding one of the plurality of sub-blocks being nearest to the preliminary position of the corresponding one of the at least one pin thereof.

24. The system as in claim 23, the means for providing the block placement representation comprising the means for providing the block placement representation generated by an optimization algorithm applied to the IC design.

25. The system as in claim 23, the means for providing the block placement representation comprising the means for providing the block placement representation generated by a genetic algorithm applied to the IC design.

26. The system as in claim 23, the means for positioning each of the at least one pin of each sub-block at a preliminary pin position along the block boundary of the block comprising:

means for obtaining a net of the IC design, the net being descriptive of at least one electrical path and signal passage thereon between one source pin and at least one sink pin, the source pin being one of the at least one pin of one

of the plurality of sub-blocks and each of the at least one sink pin being one of the at least one pin of one of the plurality of sub-blocks;

means for finding a center of mass from the at least one sink pin;

means for positioning the source pin to a position on the block boundary of the block having the shortest distance from the center of mass of the at least one sink pin; and

means for positioning each of the at least one sink pin at a position on the block boundary of the block having the shortest distance from the position of the source pin,

wherein the preliminary position of each of the at least one pin of each of the plurality of sub-blocks is established in response to the source pin and the at least one sink pins being positioned.

27. The system as in claim 26, the means for obtaining a net of the IC design comprising the means for identifying at least one critical pin of the IC design, each of the at least one critical pin being associated with one of the at least one electrical path having a specific timing budget.

28. The system as in claim 23, the means for determining at least one sub-block placement parameter comprising:

means for determining at least one of the orientation, the center of mass and the weight of the at least one pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof to thereby determine the at least one sub-block placement parameter of one of the plurality of sub-blocks therefrom.

29. The system as in claim 28, the means for determining at least one of the orientation, the center of mass and the weight of the at least one pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof comprising:

means for determining the weight of the at least one pin from the quantity of the at least one pin of the corresponding one of the plurality of sub-blocks.

30. The system as in claim 29, the means for determining the weight of the at least one pin from the quantity of the at least one pin of the corresponding one of the plurality of sub-blocks comprising the means for determining the weight of the at least one critical pin from the quantity of the at least one critical pin of the corresponding one of the plurality of sub-blocks, each of the at least one critical pin being associated with an electrical path having a specific timing budget, the electrical path being described in a net of the IC design.

31. The system as in claim 28, the means for determining at least one of the orientation, the center of mass and the weight of the at least one pin of the corresponding one of the plurality of sub-blocks obtained from the positional arrangement thereof comprising:

means for bounding the at least one pin of each of the plurality of sub-blocks with a rectangle having an area, wherein the area of the rectangle being dimensioned for bounding the at least one pin of each of the plurality of sub-blocks is minimised; and

means for determining the angle between the longest side of the rectangle of each of the plurality of sub-blocks and the horizontal axis of the block to thereby determine the orientation of the at least one pin of the corresponding one of the plurality of sub-blocks, and the orientation of the at least one pin being one of horizontal, partially horizontal, vertical, and partially vertical.

32. The system as in claim 23, the means for rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks comprising:

means for determining a rearrangement sequence based on the determined at least one placement parameter of each of the plurality of sub-blocks; and

means for sequential altering the dimensions of one of the plurality of sub-blocks to facilitate repositioning of the corresponding one of the plurality

of sub-blocks within the block boundary of the block in accordance with the rearrangement sequence.

33. The system as in claim 23, the means for rearranging the plurality of sub-blocks within the block boundary in accordance with the determined at least one sub-block placement parameter of each of the plurality of sub-blocks comprising:

means for selecting a block partition for the block, the block partition being one of a vertical block partition comprising a left block portion and a right block portion, and a horizontal block partition comprising a top block portion and a bottom block portion;

means for calculating a sub-block placement value for each of the plurality of sub-blocks based on the at least one sub-block placement parameter thereof, the sub-block placement value being algorithmically dependent upon the selected one of the top, bottom, left and right block partitions; and

means for selecting one of the plurality of sub-blocks for placement within the one of the top, bottom, left and right portions that the sub-block placement value of the selected one of the plurality of sub-blocks is algorithmically dependent upon, the selected one of the plurality of sub-blocks having the highest sub-block placement value.